Abstract

An input circuit, in particular for a multiplexer, for phase controlling of a data input signal with a clock signal, comprises a flip-flop (1), wherein the data signal is fed to a clock input of the flip-flop and the clock signal is fed to the data input of the flip-flop, and wherein the data output of the flip-flop is used as a control signal of a locked loop. An advantage of the invention is, that it is of simple design which makes the invention especially useful for high frequencies. The data output of the flip-flop is dependent on the phase relationship of the data input signal with respect to the clock signal.